EE 2501 / 001 F1 – Digital Logic Design – Summer 2013

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Office Hours: 12:00-1:00 MWF, 2:00-3:00 TH, 5:00-6:00 MW, or by appointment
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Location: Q 216 (lab Q243)
Meeting times: MTWR 11:00-11:50 am
Start Date: 05/20/2013
Pre-requisites: EE 2301 Circuit Analysis I
Textbook: A. Marcovitz, *Introduction to Logic Design*, 3rd edition, McGraw-Hill

Course Catalog Description:

This course is a study of digital circuit fundamentals with an emphasis on combinational and sequential logic design, Boolean algebra and switching theory, logic simplification and implementation using standard digital IC's of various logic families and programmable logic devices. A significant emphasis is placed on the study of digital design principles with emphasis on the use of LSI, MSI, and SSI circuits in the application and design of complex digital systems with a detailed examination of CMOS and TTL at the transistor level. Laboratory exercises reinforce theoretical concepts presented in the lecture utilizing an industry standard micro controller.

Learning Outcomes:

- Realize a Boolean expression with DeMorgan equivalent gates.
- Simplify Boolean expressions in product-of-sums (POS) and sum-of-products (SOP) forms.
- Use multiplexers and decoders in designing combinational systems.
- Implement latches and registers for designing state machines.
- Design sequential circuits using flip flops.
- Express signed, unsigned, fixed-point values in binary representations.
- Perform signed and unsigned addition and subtraction, observing errors.
- Design memory arrays using a basic static or dynamic memory cell.

Topics Covered Include:

- Boolean expression with DeMorgan equivalent gates
- Product-of-sums (POS) and sum-of-products (SOP) forms
- Multiplexers and decoders
- Latches and registers
- Sequential circuits using flip flops
- Signed, unsigned, fixed-point values in binary representations
- Signed and unsigned addition and subtraction
- Memory arrays

Grading Policy

Homework (15%): Homework is an essential component of the learning experience in this course. Students who successfully complete and understand all the assigned homework problems will find themselves well prepared for the written tests. The assigned homework problems will be collected during class periods as detailed in the course schedule, and about every other problem will be graded. The lowest homework problem grade for the semester will be dropped. A grade of zero will be recorded for any problem whose solution appears copied, even in part, from another source. Be sure to write the solution "in your own words" when collaborating with students from other groups on the solution method. Students who feel they are unfairly assessed a zero for copying homework may request referring the matter to be resolved by the SPSU Honor Council. The instructor may decide to refer to case to the Honor Council in especially egregious cases or when a student is involved in multiple incidences of copying.

Group exercises (10%): Most lecture periods with a reading assignment will begin with a "five-minute" group exercise. The purpose of these exercises is to stimulate learning of new material in groups of two members. Questions on group exercises will be short and generally require only that students have thoroughly read the day's reading assignment. Examples of question topics include definitions, identifying symbols or notation, and drawing/interpreting diagrams. The lowest group exercise grade for the semester will be dropped. Group exercises are graded out of 4 points, and any honest attempt at answering the question will receive at least 2 points.

Laboratories (15%): The results of exercises conducted during laboratory sessions in groups will be submitted in the form of lab reports. Some reports will be of professional quality where 80% of the grade is based on content, 10% on the impression of layout and formatting, and 10% on the quality of the writing. Other exercises will be submitted as informal reports where formatting is unimportant, i.e. these report are similar to the quality of a homework submission. All lab reports will be weighted equally.

Tests (3×15%): Three in-class tests will be used to assess progress in the course. Tests are comprised of problems similar to those assigned as homework or worked in class. Neither calculators nor equations sheets will be allowed on the tests. A table of powers of 2 and block diagrams of necessary MSI circuits will be provided on the test and made available in advance of the test. The tests, in general, will be curved in an attempt to maintain an overall class average of a mid C.

Final exam (15%): The format of the comprehensive final exam will be similar to that of the other tests but twice as long in length. Content covered in the class after the last test will be emphasized. The final exam will be scheduled during the standard final exam period. A student may choose, before taking the final exam, to replace their lowest test score with the final exam grade.

The scale for the final course grade is as follows:

A	90-100
B	80-89
C	70-79
D	60-69
F	0-59

Attendance Policy

Forcing everyone to come to every lecture is not practical. Each student bears responsibility for material covered in class. If you choose to miss class, that is your decision. However, completion of group exercises goes hand-in-hand with attendance. Note also that late arrival to class will result in working alone on group exercises. Homework can be scanned and emailed to the instructor if attendance during class is not possible on the due date. Everyone is expected to attend every laboratory session to receive

a non-zero grade for material covered. In general, late assignments are not accepted nor can make-up tests or laboratories be administered. Extenuating circumstances can result in exceptions to this rule, but agreement must be reached with the instructor in advance of the assignment or test which will be missed.

Academic Misconduct

At SPSU, academic misconduct is defined as "any act that could have resulted in unearned advantage or that interferes with the appropriate academic progress of others". All acts of academic misconduct will be reported to the Honor Council. For more information see www.spsu.edu/honorcode. The application of the definition of academic misconduct for each category of assignment in this course is describes as follows:

Discussion of homework problems among peers and even other sources is wholeheartedly encouraged. A single homework submission is allowed for groups of no more than two members. Note, however, that this submission must be a reflection of the group's work alone. Multiple submissions may appear similar if the same solution process is followed, but they may not be copied, not even in part. Be aware that copying of any kind from any source, including clandestine solution manuals, will be considered a violation of academic integrity. If you have a copy of the solution manual, you are strongly recommended to delete it. Using the solution manual as a crutch when solving homework is detrimental to your learning, and the temptation is great to rely heavily on it when rushed to complete a homework set. The majority of reported academic integrity violations in this course result from students copying from the solution manual. Additionally, possession of the solution manual is unnecessary as you will be provided with detailed solutions of all homework problems after they are due, as well as for non-assigned problems upon request.

Collaboration among group members during group exercises is obviously encouraged, but assistance of any kind from outside the group will be considered a violation of academic integrity.

Tests and the final exam are to be reflections of the individual's work alone. Assistance of any kind, including notes, calculators, cell phones, etc. will be reported as a violation to the Honor Council.

Disability Statement

If you have a documented disability as described by the Rehabilitation Act of 1973 and the Americans with Disabilities Act (ADA) that may require you to need assistance attaining accessibility to instructional content to meet course requirements, please contact the ATTIC at 678-915-7361 as soon as possible. It is then your responsibility to contact and meet with the instructor. The ATTIC can assist you and the instructor in formulating a reasonable accommodation plan and provide support for your disability. Course requirements will not be waived but accommodations will be made, when appropriate, to assist you to meet the requirements.

Communication

Course material will be disseminated in D2L including lecture notes and recordings, homework solutions, old tests, etc. All official course announcements, including instructions when class may be cancelled, will be posted in the D2L course news. Be sure to check D2L regularly.

Course Schedule

Day	Date	Description	Reading	Homework due
Mon	05/20	1 Introduction and number systems	1.1-1.2.1	
Tue	05/21	2 Codes and binary arithmetic	1.2.2-1.2.6	
Wed	05/22	3 Two's complement		
Thu	05/23	4 Truth tables and switching algebra	2.1-2.2, 2.6	
Tue	05/28	5 Circuit synthesis	2.3-2.5, 2.9	
Wed	05/29	6 Transistor switching		
Thu	05/30	7 Logic gate circuitry		1.1, 1.4, 1.8, 1.9, 2.2c, 2.3, 2.13, 2.26c,e
Mon	06/03	8 K-maps	3.1-3.2, 3.4	
Tue	06/04	9 K-map extensions	3.3, 3.5-3.6	
Wed	06/05	10 Quine-McCluskey	4.1, 4.3-4.4	
Thu	06/06	Review		3.1a,c, 3.5a,b,d, 3.9a,b, 3.12a,c, 4.1a,c, 4.4a
Mon	06/10	Test 01		
Tue	06/11	11 Iterative systems	5.1	
Wed	06/12	12 Decoders and encoders	5.2-5.3	
Thu	06/13	13Multiplexers and demultiplexers	5.4	
Mon	06/17	14 Three-state gates	5.5	
Tue	06/18	15 Gate arrays	5.6	
Wed	06/19	16 Verilog	5.7	
Thu	06/20	17 Larger iterative systems	5.8	5.3, 5.5, 5.8, 5.11, 5.13, 5.98[1], 5.99[2]
Mon	06/24	Review		5.100[3]
Tue	06/25	Test 02		
Wed	06/26	18 Sequential circuits	6.1	
Thu	06/27	19 Latches and flip-flops	6.2-6.3	
Mon	07/01	20 Sequential systems	6.4	
Tue	07/02	21 Sequential design	7.1	
Wed	07/03	Recitation		
Mon	07/08	22 Counters	7.2-7.3	6.1a, 6.3c, 6.5a, 6.8a, 7.1, 7.2ia[4]
Tue	07/09	23 State machine design	7.4	
Wed	07/10	Review		7.8dii, 7.16o
Thu	07/11	Test 03		
Mon	07/15	24 Registers	8.1-8.2	
Tue	07/16	25 PLDs	8.3-8.4	
Wed	07/17	26 One-hot encoding	8.5	
Thu	07/18	27 Verilog for sequential systems	8.6	
Mon	07/22	28 Memory arrays		
Tue	07/23	29 A simple computer	8.7	
Wed	07/24	Recitation		8.2, 8.5b, 8.99[5]
Thu	07/25	Review		
???	07/31	Final exam		

This course schedule is subject to modification depending on the pace of the course. However, homework assignments and test dates will not be changed unless students anonymously and unanimously vote for a change.

[1] Using only 74x151 multiplexers , design a 2-to-1 multiplexer where each of the two inputs contains 4-bits each.
[2] Design a single bit 4-to-1 multiplexer using only one 74x139 decoder and any number of three-state gates.
[3] Configure a PAL to implement an 4-bit two's complement converter (like in problem 5.3) without a carry in or out. That is specify the rows and columns of fuses that must be blown or left intact, including those on the XOR outputs (see the image file under the syllabus for the PAL layout on D2L). Compare the delay of this device to the one in problem 5.3.
[4] Also include the block/circuit diagram using D flip flops.
[5] Design a counter to go through the sequence 3, 1, 2, 0 and repeat, and implement it in a GAL (see GAL file under the syllabus on D2L).

Laboratory Schedule

Day	Date	Description
Mon	05/20	Make-up of missed lecture hours
Mon	06/03	Introduction to Logic Gates
Mon	06/10	Switches and LEDs in Logic Circuits
Mon	06/17	Seven-segment display
Mon	06/24	Seven-segment display continued
Mon	07/01	Adders
Mon	07/08	Adders continued
Mon	07/15	Rolling the dice
Mon	07/22	State machine design